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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,254	02/11/2004	Hiroshi Iwata	0397-0475P	9897

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,254	IWATA ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,8-10,12,15-17,21 and 22* is/are rejected.

7)☒ Claim(s) *6,7,11,13,14,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The amendment submitted by Applicant on February 21, 2006 has been received and entered.

2. Claims 1-2 and 4-22 are pending.

Claim 3 has been canceled.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-5, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Morii (U.S. Patent No. 5,424,979).

Regarding claim 1, Morii disclosed in Figures 1(b)-1(c) a non-volatile memory cell of a side wall accumulation type comprising an n-type source region [24] and an n-type drain region [25] facing each other, and a channel region [unnumbered] positioned between the source region [24] and the drain region [25]. The source region [24] and the drain region [25] are provided in the upper portion of a p-type substrate [11] (column 8, lines 28-34). On the substrate [11], a gate insulating film is provided and includes three portions [13a], [13b], [13c] over the source region [24], the drain region [25] and the channel region, respectively (column 8, lines 41-59). A first floating gate [17a] is provided on the first portion [13a], and a second floating gate [17b] is provided on the second portion [13b]. As shown in Figure 1(b}, the first and second floating gates [17a], [17b] are on both side of a control gate [14] (column 8, line 63), and the floating gates [17a], [17b] are overlapping part of the source region [24] and the drain region [25].

Although Morii did not discuss the amplifier, however, it is conventional that the memory cells in memory device are coupled to sense amplifier for memory access operation.

Regarding claim 2, it is conventional that on or more transistors of peripheral circuits are connected in series to the memory cell.

Regarding claims 4-5, as shown in Figure 1(b}, the floating gates [17a], [17b] having the side and bottom disposed adjacent to the insulating films [13a], [13b] and [12], where the side and the bottom edges of the floating gates [17a], [17b] are parallel to the insulating films.

Regarding claims 8-9, the memory cells disclosed by Morii would be used in any electronic device.

5. The indicated allowability of claims 10-22 is withdrawn in view of the newly discovered reference(s) to Ma et al. (U.S. Patent No. 6,714,454). Rejections based on the newly cited reference(s) follow.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 10, 12, 15-17, 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (U.S. Patent No. 6,714,454).

Ma et al. disclosed in Figure 3 a double-polysilicon dual bit cell structure [300] includes a select gate [301] extending over at least a portion of two adjacent floating

gates [303A], [303B] (column 5, lines 34-36, 49-52). Cell structure further includes a right junction [304], a left unction [305], and a channel region therebetween. Junctions [304] and [305] serve interchangeably as the cell's drain and source terminals (column 5, lines 64-67). A gate-oxide layer [310A] separates floating gate [303A] from the right junction [304] and channel section [3131]. Similarly, a gate-oxide layer [310B] separates floating gate [303B] from the left junction [305] and the channel section [315] (column 6, lines 14-18). As shown in Figure 3, the right junction [304] and the left junction [305] are formed in a body (substrate) [306 (column 6, line 44). Although Ma et al. did not discuss the conductivity types of the body [306] and the left and the right junctions [305], [304], it is conventional that their conductivities are opposite to the other. Also, Ma et al. did not discuss the amplifier, it is conventional that memory cells in memory device are connected to amplifier for memory access operations.

Regarding claim 12, Ma et al. showed in TABLE 3 (column 9) different states of the Left-bit and the Right-bit. As the possible states of the Left-bit is "0" or "1" then the state of the Right-bit is "0".

Regarding claims 15, it is conventional that on or more transistors of peripheral circuits are connected in series to the memory cell.

Regarding claims 16, Ma et al. showed in Figure 3 the floating gates [303A] overlaps part of the right junction [304], and the floating gate [303B] overlaps part of the left junction [305].

Regarding claim 17, as the floating gates [303A] and [303B] considered as film having the function of retaining charges, the bottom of the floating gates [301A] and [303B] are parallel to the Gate-oxide layer [310A], [310B].

Regarding claims 21-22, the memory cells disclosed by Ma et al. would be used in any electronic device.

8. Claims 6-7, 11, 13-14, 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

10. **REMARKS**

A new 35 U.S.C. 102(b) rejection based on new references to Morri and Ma et al. that recited the features in claims 1-2, 3-4, 8-9, 10, 12, 15-17 and 21-22.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arakawa, Amin et al., Kohda et al., and Pan are cited to show memory devices having floating gates on both sides of a gate..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
March 08, 2006